

ARCHITECTURE-AWARE TRANSACTION SCHEDULING METHODOLOGY IN HIGH-LOAD BLOCKCHAIN NETWORKS

Vinnitsia National Technical University, Ukraine

Abstract

The paper addresses the issue of Hyperledger Besu blockchain node performance degradation in high-load networks caused by the State Bloat phenomenon. An architecture-aware transaction scheduling methodology, RATEM, is proposed based on prefix-based request clustering to optimize Last Level Cache (LLC) utilization. The mechanisms of interaction between the proposed method, the JVM runtime environment, and hardware prefetching units are substantiated. Theoretical analysis indicates a potential 10–15% reduction in average RPC request processing latency.

Keywords: Blockchain, Hyperledger Besu, Merkle Patricia Trie, L3 cache, transaction scheduling, architecture-aware method, JVM.

Introduction

Modern decentralized systems are shifting from network-bound to memory-subsystem-bound constraints. Under high load, the "State Bloat" phenomenon leads to significant node performance degradation [1]. Traditional transaction scheduling in mempools treats computing resources as static parameters, ignoring internal processor architecture, specifically L3 cache capacity limitations. This necessitates developing methods to improve cache utilization efficiency when processing large state trees. The Merkle Patricia Trie (MPT) used for state storage is a 16-ary prefix tree [1]. Data access operations are classified as "Pointer Chasing," which is inherently inefficient for pipelined processors due to memory address unpredictability. For modern architectures, the total request processing time T_{total} is modeled as:

$$T_{total} = T_{exec} + \sum_{i=1}^n (L_{miss} \cdot P_i)$$

Where T_{exec} is instruction time, N is tree depth, L_{miss} is DRAM latency, and P_i is the miss probability at the i -th level. Optimizing requires specific input data organization to ensure the reuse of tree nodes already residing in the cache [3].

Proposed RATEM Method

Proposed RATEM Method. The RATEM (Resource-adaptive Architecture-oriented Transaction Execution Method) transforms the mempool queue to maximize both temporal and spatial data locality during execution. Instead of standard FIFO or gas-price-based ordering, RATEM introduces a multi-layered scheduling approach:

- **Prefix-based Clustering:** Transactions are grouped by common recipient address prefixes (nibbles). Since the MPT is a prefix-based structure, the upper levels of the tree (branch nodes) are shared among addresses with similar starting characters. Clustering allows these nodes to be loaded into the L3 cache once and reused for the entire batch, effectively software-mitigating the impact of tree depth on latency [2].
- **Adaptive Scheduling Window:** The batch size is dynamically adjusted based on the hardware's available L3 cache capacity to prevent "cache pollution" by heterogeneous data that lacks shared access paths.

- **Node Traversal Optimization:** By prioritizing transactions that target "hot" state branches, the method ensures that the most frequently accessed segments of the MPT remain in the Last Level Cache (LLC), minimizing the penalty of DRAM access [1].

Interaction with the JVM Runtime

Implementing RATEM for blockchain clients like Hyperledger Besu must account for the Java Virtual Machine (JVM) virtualization layer. [3] Although the JVM abstracts physical address management, the methodology exploits heap object placement and JIT compiler behaviors:

- **Heap Locality:** By processing clustered transactions sequentially, the methodology increases the likelihood that related MPT node objects are allocated in contiguous memory regions within the Young Generation, facilitating better cache line utilization [4].
- **Hardware Prefetcher Stimulation:** Sequential iteration through similar tree branches creates a predictable access pattern that stimulates the hardware prefetching units. This enables the CPU to fetch necessary branch nodes from RAM into the L3 cache before the JVM initiates the actual read operation, neutralizing the "pointer chasing" latency [5].

Conclusions

The scientific novelty of this research lies in formalizing the link between the hierarchical Merkle Patricia Trie structure and the dynamics of Last Level Cache (LLC) utilization to minimize state access latency. This approach moves beyond generic software optimization by incorporating architecture-specific memory hierarchy traits into the transaction execution flow. Experimental validation is planned using advanced processor architectures with expanded L3 cache (such as 3D-stacked memory) to confirm the hypothesis regarding the critical impact of cache volume on node stability under extreme loads. Theoretical analysis indicates that the implementation of the RATEM methodology can reduce average RPC request latency by 10–15% without necessitating changes to the underlying consensus protocol

References

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Maksym Bystryk – Ph.D Student of Software Engineering, Vinnytsia National Technical University, Vinnytsia, email: max.bystryk@gmail.com

Oleksandr Khoshaba - Ph.D., Associate Professor of Software Engineering, Vinnytsia National Technical University, Vinnytsia, e-mail: oleksandr.khoshaba@gmail.com